SIEMENS

8M × 32 -Bit Dynamic RAM Module — HYM 32V8040GD(L)-50/-60
SMALL OUTLINE MEMORY MODULE

Preliminary Information

- 72-Pin Small Outline Dual-in-Line Memory Module
- 2 bank 8M x 32-bit organization
- Fast Page Mode Operation
- Performance:

		-50	-60	
t_{RC}	Read / Write Cycle Time	90	110	ns
t_{RAC}	$\overline{RAS}$ Access Time	50	60	ns
t_{CAC}	$\overline{CAS}$ Access Time	13	15	ns
t_{AA}	Access Time From Address	25	30	ns
t_{PC}	Fast Page Mode Cycle Time	35	40	ns

- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 936 mW active (-50 version)
  max. 756 mW active (-60 version)

  LVTTL - 28.8 mW
  LVCMOS– 13.0 mW standby
  LVCMOS– 5.76 mW standby (L-version)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh
- Self Refresh on HYM32V8040GDL versions
- 4 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- Card Size 59.69mm x 25.40mm x 3.80mm
- Utilizes four 4M × 16 -DRAMs (HYB 3165160AT(L)) in 400 mil wide TSOPII-50 packages
- 12R / 10C addressing
- 4096 refresh cycles / 64 ms for HYM32V8040GD
  4096 refresh cycles / 256ms for HYM32V8040GDL
- Gold contact pad

The HYM 32V8040GD(L) -50/-60 is a 32 MByte DRAM module organized in 2 banks by 4M by 32-bit in a 72-pin, dual read-out, small outline package comprising four HYB 3165160AT 4M × 16 DRAMs in 400 mil wide TSOPII-50 - packages mounted together with four ceramic decoupling capacitors on a PC board. Each HYB 3165160AT is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed. The HYM32V8040GDL (L-versions) have a very low power „sleep mode“ supported by Self Refresh

The density and speed of the module can be detected by the use of presence detect pins.

These modules are ideal for portable systems applications where high memory capacity is needed.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 32V8040GD -50	Q67100	L-DIM-72-4	50 ns DRAM module
HYM 32V8040GD -60	Q67100-	L-DIM-72-4	60 ns DRAM module
HYM 32V8040GDL -50	Q67100	L-DIM-72-4	50 ns Low Power DRAM module with Self Refresh
HYM 32V8040GDL -60	Q67100-	L-DIM-72-4	60 ns Low Power DRAM module with Self Refresh

Pin Names

A0-A11	Row Address Input
A0-A9	Column Address Inputs
DQ0 - DQ31	Data Input/Output
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read / Write Input
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD7	Presence Detect Pins
N.C.	No Connection

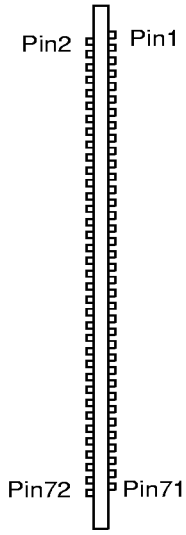
Presence-Detect Truth Table *):

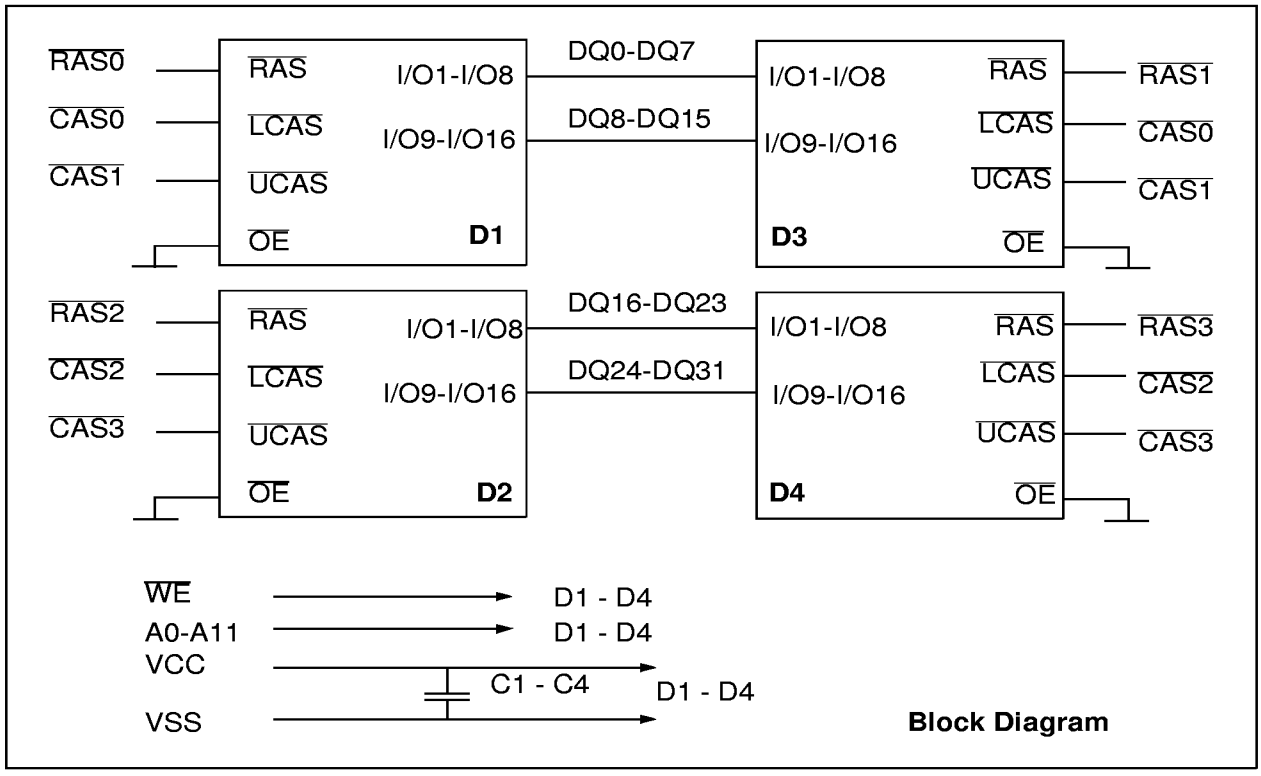
Module	PD1	PD2	PD3	PD4	PD5	PD6	PD7
HYM 32V8040GD -50	NC	NC	VSS	VSS	VSS	VSS	NC
HYM 32V8040GD -60	NC	NC	VSS	VSS	NC	NC	NC
HYM 32V8040GDL -50	NC	NC	VSS	VSS	VSS	VSS	VSS
HYM 32V8040GDL -60	NC	NC	VSS	VSS	NC	NC	VSS

Pin Configuration

PIN	Name	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	37	DQ16	2	DQ0	38	DQ17
3	DQ1	39	VSS	4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	$\overline{CAS2}$	6	DQ4	42	$\overline{CAS3}$
7	DQ5	43	$\overline{CAS1}$	8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	$\overline{RAS1}$	10	VCC	46	NC
11	PD1	47	$\overline{WRITE}$	12	A0	48	NC
13	A1	49	DQ18	14	A2	50	DQ19
15	A3	51	DQ20	16	A4	52	DQ21
17	A5	53	DQ22	18	A6	54	DQ23
19	A10	55	NC	20	NC	56	DQ24
21	DQ8	57	DQ25	22	DQ9	58	DQ26
23	DQ10	59	DQ28	24	DQ11	60	DQ27
25	DQ12	61	VCC	26	DQ13	62	DQ29
27	DQ14	63	DQ30	28	A7	64	DQ31
29	A11	65	NC	30	VCC	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	$\overline{RAS3}$	69	PD5	34	$\overline{RAS2}$	70	PD6
35	DQ15	71	PD7	36	NC	72	VSS

Front Side **Back Side**





Absolute Maximum Ratings [1)]

Operating temperature range.....0 to 70 °C
Storage temperature range.....– 55 to 150 °C
Input/output voltage.....-0.5 to min (Vcc+0.5,4.6) V
Power supply voltage.....-0.5V to 4.6 V
Power dissipation.....1.2 W
Data out current (short circuit).....50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1)
Input low voltage	V_{IL}	– 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage (Iout = -2mA)	V_{OH}	2.4	–	V	1)
Output low voltage (LVTTL) Output „L“level voltage (Iout = +2mA)	V_{OL}	–	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ level voltage (Iout = -100uA)	V_{OH}	Vcc-0.2	-	V	1)
Ouput low voltage (LVCMOS) Output „L“ level voltage (Iout = +100uA)	V_{OL}	-	0.2	V	!)
Input leakage current,any input (0 V < Vin < Vcc , all other pins = 0 V	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DO is disabled, 0 V < $Vout$ < Vcc)	$I_{O(L)}$	– 10	10	µA	
Average Vcc supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC min.)	I_{CC1}	 – –	 260 210	 mA mA	2) 3) 4)
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= Vih)	I_{CC2}	–	8	mA	–
Average Vcc supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = VIH: tRC = tRC min.)	I_{CC3}	 – –	 260 210	 mA mA	2) 3)

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average *V*cc supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: tPC=tPC min.)	I_{CC4}	– –	120 100	mA mA	2) 3) 4)
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= *V*cc-0.2V)	I_{CC5}	–	3.6 0.8	mA mA	– L-version
Average Vcc supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: tRC = tRC min.)	I_{CC6}	– –	260 210	mA mA	2) 4)
Self Refresh Current (L-version) (CBR cycle with tRAS>tRASSmin, $\overline{CAS}$ held low, $\overline{WE}$=Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V	I_{CC7}	–	1.6	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,$\overline{WE}$)	C_{I1}	–	25	pF
Input capacitance ($\overline{RAS0}$- $\overline{RAS3}$)	C_{I2}	–	20	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	20	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	15	pF

AC Characteristics [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
common parameters							
Random read or write cycle time	t_{RC}	90	–	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10k	15	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45		
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	30	3	30	ns	7
Refresh period	t_{REF}	–	64	–	64	ms	
Refresh period for L- version	t_{REF}	–	256	–	256	ms	
Read Cycle							
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8,10
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12

AC Characteristics (cont'd) [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 5 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Early Write Cycle							
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	13
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	14
Data hold time	t_{DH}	10	–	10	–	ns	14
Fast Page Mode Cycle							
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	30	–	35	ns	7
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle							
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	ns	
Self Refresh Cycle (L-version only)							
$\overline{RAS}$ pulse width	t_{RASS}	100k	_	100k	_	ns	15
$\overline{RAS}$ precharge time	t_{RPS}	95	_	110	_	ns	15
$\overline{CAS}$ hold time	t_{CHS}	-50	_	-50	_	ns	15

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate and specified per module bank

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume tT = 5 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with a load equivalent to 2 TTL loads and 100 pF.

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels

13) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle.

14) These parameters are referenced to the $\overline{CAS}$ leading edge.

15) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
If row addresses are being refresh in an evenly distributed manner over the refresh iterval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh.

SO-DIMM PACKAGE OUTLINES